

## POWER AMPLIFIER 1KW LOW BAND 40D1137G1,2

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## **POWER AMPLIFIER 1KW LOW BAND 40D1137G1,2**

### **1 FUNCTIONAL DESCRIPTION**

The Power Amplifier module consists of a four-way power splitter, four 250 W FET amplifiers, a four-way power combiner, a VSWR protection board, and power & I/O connectors. Two full-size heatsinks provide the cooling for the active devices. It is designed for 1 kW sync peak power output in Low Band 54 - 88 MHz analog television systems, and provides power gain of approximately 20 dB, with 1 kW peak sync visual or 600 W aural output. The module can provide upwards of 200W of average digital power when used with appropriate predistortion. It is fully hot-pluggable, incorporating protective circuitry for excess VSWR power cutback.

## 2 4-WAY SPLITTER/INPUT BOARD

Part Number: 40D1209G1/40D1209G2

References: Figure 4 and Figure 5.

The 4-Way splitter receives its RF input signal from the drive stage and provides input signals to the four FET amplifiers. The incoming signal is first split in two by a Wilkinson splitter and the two resultant signals are split again by two more 2-way Wilkinson splitters to provide the four outputs required. Balance terminations are provided by R1, R2, and R3, and trimmed by reactive elements C1-C6 and L1.

A built-in detector (CR1 and C7) is fed from a directional coupler on the input transmission line. This detector provides a sample of the input signal for module gain monitoring. The directional coupler is terminated by R4.

### 3 FET RF AMPLIFIERS

References: Figure 6, Figure 7, Figure 8.

Each of the four amplifiers consists of two, source grounded, N-channel, insulated gate Field Effect Transistors (FETs) packaged in a single case and operating Class AB in a push-pull configuration. Because these FETs are "enhancement mode" devices, they require a positive gate-to-source bias voltage on each gate to cause source-drain conduction. The quiescent Class AB idling bias current is set independently for each half. The gate voltage required to produce this idling current may vary between 2 V and 5 V according to the device specification sheet, and the idling current used. FET gate threshold voltages also are temperature sensitive, so thermal compensation is provided by RT1 and RT2. Bias current is set to 500mA per half of the device for analog operation and 750mA per half for digital operation.

The gate voltage is applied through an adjustable voltage divider from this +39 V regulated bias rail. Resistors R1, R2, R3 and R4 provide gate bias for one half of the amplifier; R5, R6, R7 and R8 provide bias for the other half.

The input signal is applied to balun T1 to provide two signals 180° out of phase. These signals are stepped down to match the low input impedance of the device through a pi-network consisting of C1, C2, L1, L2, C4, and the device C<sub>G-S</sub>. The gate input impedance at the operating frequency is low compared with the values of R3 and R6, so these resistors have no effect at RF.

R3 and R6 provide a DC path for bias, and provide loading at lower frequencies to assist in maintaining amplifier stability. The choice of C6, C7, C20, C21 values, and internal equivalent series impedances, also ensures effective bypassing at all frequencies of interest.

The output matching pi-network, consisting of inductors L3 thru L9, and capacitances C13 thru C16, tunes out the FET drain capacitance and transforms the very low output impedance of the FET to 12.5 ohms. The two antiphase output signals are combined in balun T2, L9. The electrical lengths of L7 and L8 are adjusted for the low band coverage split that takes effect at about 75 MHz, by the placing of jumpers on part of the length of each inductance, for channels 5 and 6.

DC is applied to the drains through L3, L4 for the first half, and L5, L6 for the other half. L3 and L6 are also short sections of microstrip transmission line which transform the impedances of C9 and C11 to more effective values as seen by the FET. RF and lower frequencies are bypassed with paralleled C5, C9, C10 for one half of the amplifier, and C8, C11, C12 for the other half. These groups of capacitors are selected in value and for their internal equivalent series inductances so that they will be an effective bypass at critical frequencies of interest, including video, to assist in maintaining stability.

Note that fuses are provided for the voltage supplied to the FET drain connections. The intent of these fuses is to protect the surrounding circuitry in the event of a device failure. The normal failure mode of active devices such as these is short-circuit, and the fuse will blow in this case, isolating the defective device from the rest of the module and transmitter power supply, allowing the remaining devices to keep operating normally. A blown fuse can serve as a valuable troubleshooting aid, when trying to identify failed devices.

## 4 4-WAY POWER COMBINER

Part Number: 40D1206G1

References: Figure 9 and Figure 10.

The four amplifier outputs are applied to two 2-way Wilkinson combiners and phase delayed to correct the quadrature condition imposed by the input splitter board. The two outputs of these Wilkinson combiners are combined by another two-way Wilkinson combiner into a single 50 ohm output. Terminations for the Wilkinson networks are provided by R1, C1, R2, C2, C3, L1, C4, C5, and R3, C8. There is one directional coupler, and one bi-directional coupler located at the combiner output.

A directional coupler feeds a BNC connector on the module front panel and can be used for RF output monitoring. The bi-directional coupler provides a detected sample of both the forward and reflected RF power to the VSWR protection board for monitoring module gain, and VSWR protection. Terminations for these coupler line sections are provided by R4, R5, and R6; the RF samples for VSWR monitoring are detected by CR1 and C6 for the forward direction, and by CR2 and C7 for the reflected direction.

## 5 VSWR CONTROL BOARD

Part number: 20B1549G1

References: Figure 11 and Figure 12.

The VSWR control board performs a number of functions: it provides regulated bias voltages to the FET power amplifier stages, it provides hot-plug-in capability to protect the amplifier module when plugged into an operating transmitter, it provides protection to the FETs against over-dissipation due to high VSWR, and it monitors the module RF power gain.

If the module is plugged into a powered transmitter using several modules running in parallel, the power supply connections are first made through the longer contacts of the module's DC power connector and into VSWR board J1 pin 8. This allows the electrolytic bypass capacitors of all amplifiers to charge through current limiting resistor R5, preventing overstress of all amplifier fuses due to charge current of the bypass capacitors. When the module is fully seated, the high current contacts are connected and the module can operate normally.

In normal operation the power supply enters J1 via pin 2, and is regulated to +39 VDC by series resistor R10 and zener diode VR1. Regulator U1 provides constant B+ voltage for op-amps U2, U3, U4, and the comparator reference voltages. When the module is first turned on (or plugged in) and U1 begins regulating, the charging current of C7 turns on Q1 which pulls the bias line low for a brief period of time. This provides a slow start for the module after DC power is applied.

The overall RF system of the transmitter provides overall VSWR protection via the external RF detector boards discussed in other sections of this manual, but VSWR sensing is also provided in the module for its own safety.

In the transmitters utilising modules in parallel, one or more failed or disconnected modules or a fault in the six-way combiner or subsequent 3 dB coupler, may cause a module output mismatch.

To the module, any mismatch which appears as reflected power is detected and sensed at pin 11 of J1 to comparator circuit U2B.

R21 sets the level at which VSWR protection begins. If the level of detected reflected power on pin 5 of U2B exceeds the control voltage set on pin 6, the output on pin 7 will go high. R22, C10, and CR1 provide a fast attack, slow release control voltage to Q2 when a high VSWR condition suddenly occurs. This will turn on Q2 which turns on Q4 which quickly reduces the bias applied to the power amplifier FETs; this reduced bias also reduces their gain and therefore their RF output and keeps the amplifier at safe levels.

When a module is plugged into an operating transmitter, the slow start circuitry consisting of C7 and Q1 will initially keep the module turned off. Power from the other modules working into the combiner will enter the module and be detected by the reflected power detector. This would prevent the module from ever operating properly, unless the VSWR circuit is momentarily over-ridden.

The circuit of U4 produces a pulse approximately 2 seconds after power is applied to the module. At power-up, pin 2 of U4 will be pulled high by C11. R26 charges this capacitor, and when the pin 2 voltage goes below the voltage on pin 3, the output of U4 will go high. A pulse whose duration is controlled by C9 and R18 will then be applied to pin 3 of U2A. U3B detects that the module is not producing forward power and that the reverse power is high. Under these conditions the output of U2A goes high, turning on Q3, momentarily disabling VSWR protection, and allowing the module to come on.

DC samples corresponding to forward power into and out of the module are applied to U3A pins 2 and 3 respectively. When pin 3 voltage is higher than that of pin 2, corresponding to "RF gain is okay" the comparator output U3A pin 1 is high, causing the green LED on the front panel of the module to light. The comparison threshold (ie. module gain is ok) is set by adjustment of R4.

## 6 ADJUSTMENT OF BIAS VOLTAGE TO ESTABLISH PROPER QUIESCENT FET BIAS CURRENT

**Important:** 50  $\Omega$  input *and* output terminations are necessary to achieve consistent results and prevent damage to the devices when testing modules. Supplemental cooling is not required when performing bias adjustments or low power sweep of the PA modules.

1. Remove **all** fuses from the module to be tested. (There are 8 fuses in total).
2. Adjust all bias pots to maximum resistance, for minimum bias voltage. (Again, there are 8).
3. Use a clip lead to short the junction of C7, C21, R6, and R7 to ground. This shuts off side B of the amplifier so it will not interfere with measurement of quiescent current from side A.
4. Terminate the RF input and output into a 50  $\Omega$  load.
5. Apply +50VDC from the front panel test point on the transmitter, through an ammeter, to the positive copper bus bar, and its negative to chassis. **Caution:** Observe polarity!
6. Check the voltage on the bias terminals, it should be 39 V  $\pm$ 2 V. (The bias terminals are connected together via insulated bus wire).
7. Read the current drawn by the VSWR board and bias regulator. Next, install a fuse in side A (nearest the panel) of amplifier #1; adjust the corresponding bias pot for a 500 mA increase in the power supply current; this increase corresponds to an idling bias current of 0.5 A. Remove the fuse. Remove the side B bias short and place it on side A at the junction of C6, R2, R3 and R9. Place the fuse in side B. Adjust the side B bias pot for the proper current.
8. Move the fuse to the remaining fuse holders, one at a time, and adjust each companion bias potentiometer in the same manner for the proper bias current.
9. Install remaining fuses and remove the bias short after all bias adjustments have been made.

## POWER AMPLIFIER 1KW LOW BAND 40D1137G1,2

### 7 LOW POWER SWEEP OF AMPLIFIERS

**Note:** Low power sweep of PA modules should not be required under normal circumstances – even when replacing FET devices. There are no tuning adjustments on these modules.

1. Ensure that terminations are in place in the test setup. All modules require 50  $\Omega$  source and load impedances for consistent results during testing.
2. Connect the module to a sweep system, typically as shown in Figure 1. The sweep generator should be adjusted to give a linear sweep from about 45 to 75 MHz, or from 65 to 95 MHz, to sweep the part of Low Band that the module is intended for, with a small amount of out-of-band signal on both ends. Ensure that a coaxial 20 dB attenuator pad is connected to the RF output of the amplifier, in order to prevent possible damage to the sweep comparator.
3. Connect the lab power supply +50 V to the positive supply bus bar, and the negative to the chassis of the amplifier. The current should be limited to 7 or 8 A for this test. **Caution:** observe polarity!
4. With the power supply switched on, the current drawn should be not more than the bias current for all the devices together - about 4 amperes (8 x 0.5 A) for the PA module.

The swept in-band frequency response, for Low Band modules, should be essentially flat within  $\pm 1$  dB as shown in Figure 1, with gain approximately  $20 \pm 1$  dB.

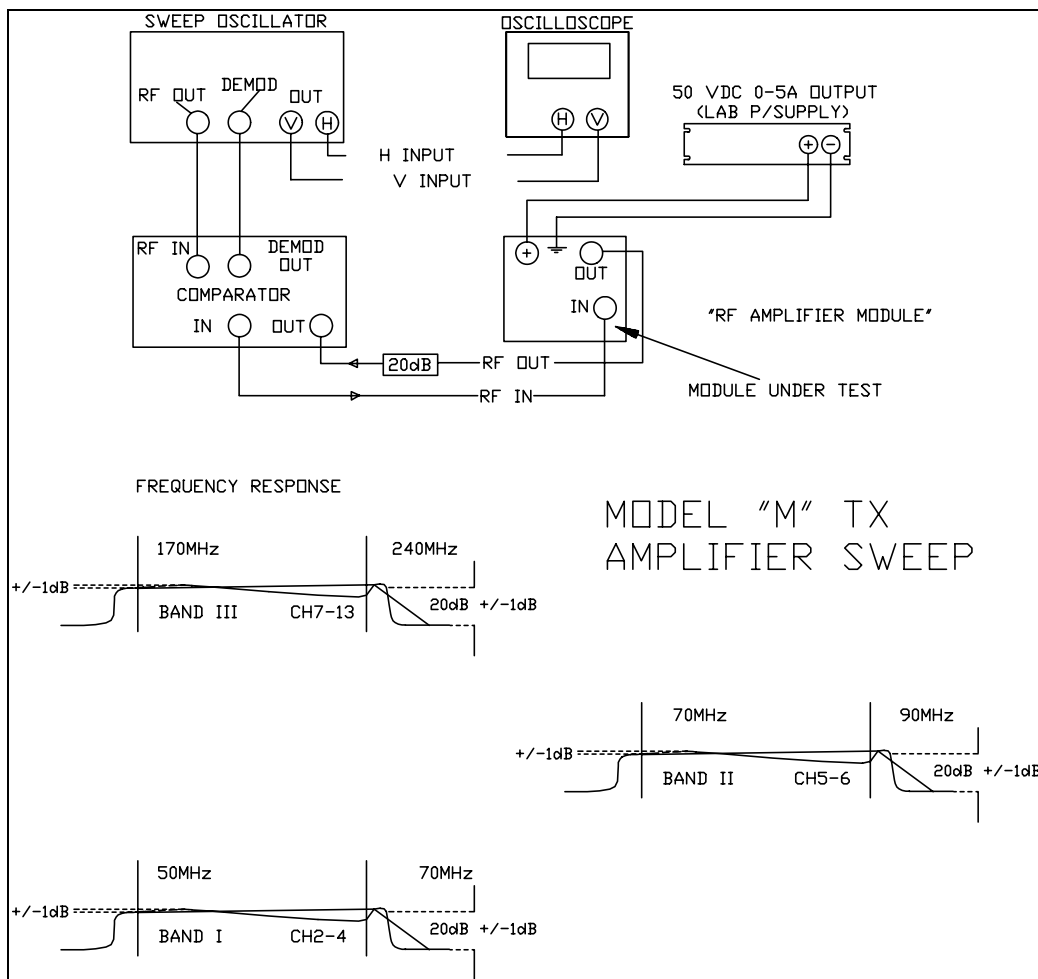


Figure 1 Module Sweep Setup



## 8 GREEN LED SENSITIVITY ADJUSTMENT

One of the functions of the VSWR board is to monitor the overall gain of the PA module. This VSWR board is located at the rear of the module, adjacent to the output RF connector. For the locations of the components on the board, please refer to Figure 11 and Figure 12.

**Verify that all the PA modules are in good working order**, and then proceed as follows:

1. With all modules running at normal operating power, place AGC/MANUAL switch into the MANUAL position and adjust the exciter output power until the transmitter output power reads 110%.
2. Remove the module to be set up, and remove the two front fuses from it, in order to simulate a single FET package failure. Replace this "crippled" module in the transmitter, and apply a nominal 50% APL staircase video signal to the transmitter (analog transmitters).

The green LED should now be extinguished; if it is not, remove the module and adjust potentiometer (R4) on the VSWR board clockwise, replace the module and try again, repeating until the LED is barely extinguished when the module is re-powered.

3. Replace the fuses so the module is again fully operational, and verify that the green LED is now fully lighted when the module is replaced in the transmitter and re-powered.

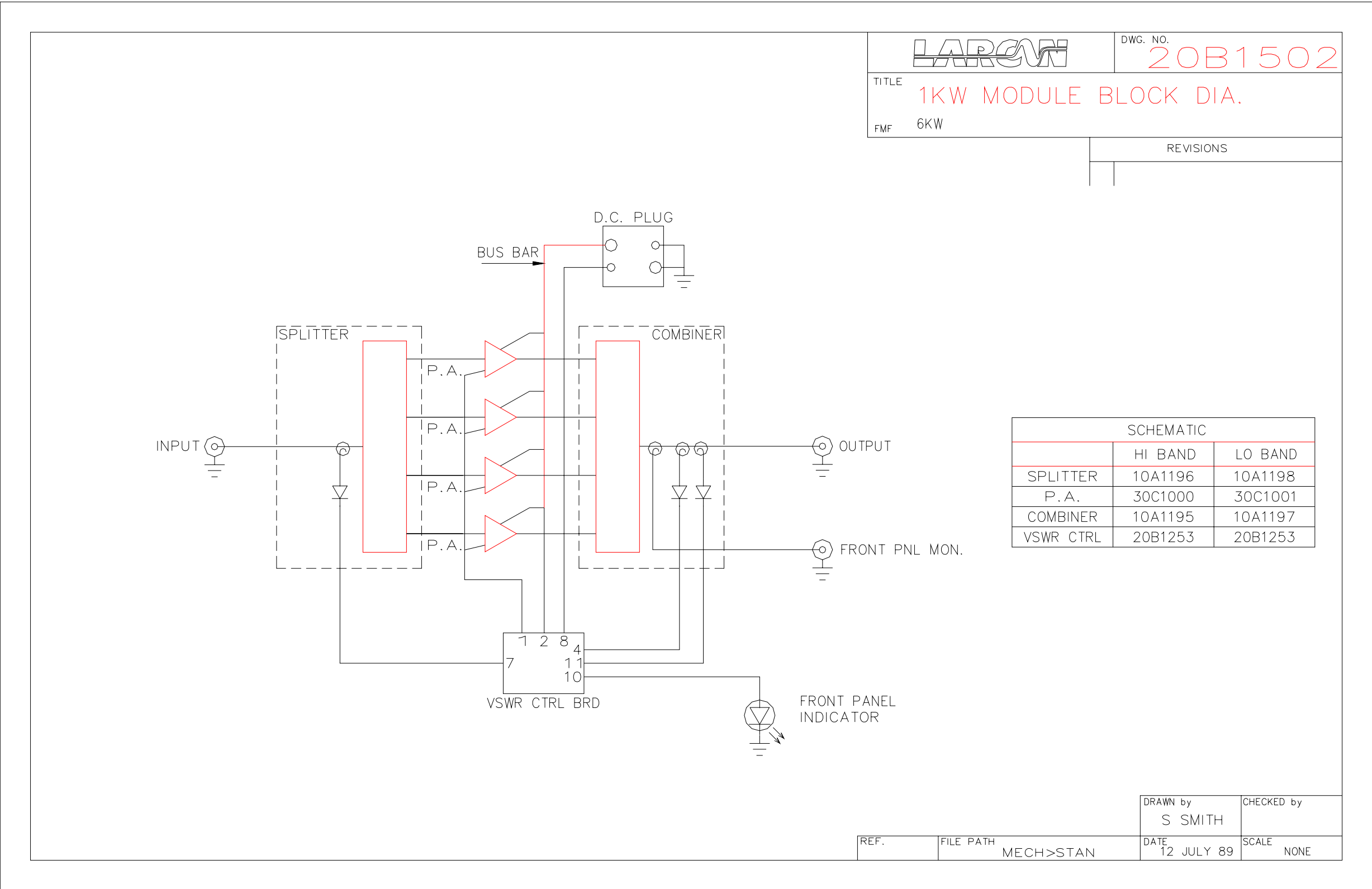
It is recommended that R4 be adjusted one half turn at a time, to establish a known reference point.

4. Place the AGC/MANUAL switch in the AGC position, and with the RAISE/LOWER switch, readjust the transmitter output power to 100%.
5. Similarly, the aural amplifier may be adjusted in the same manner, but being an FM signal the modulation of the carrier is not critical.

[illegible]

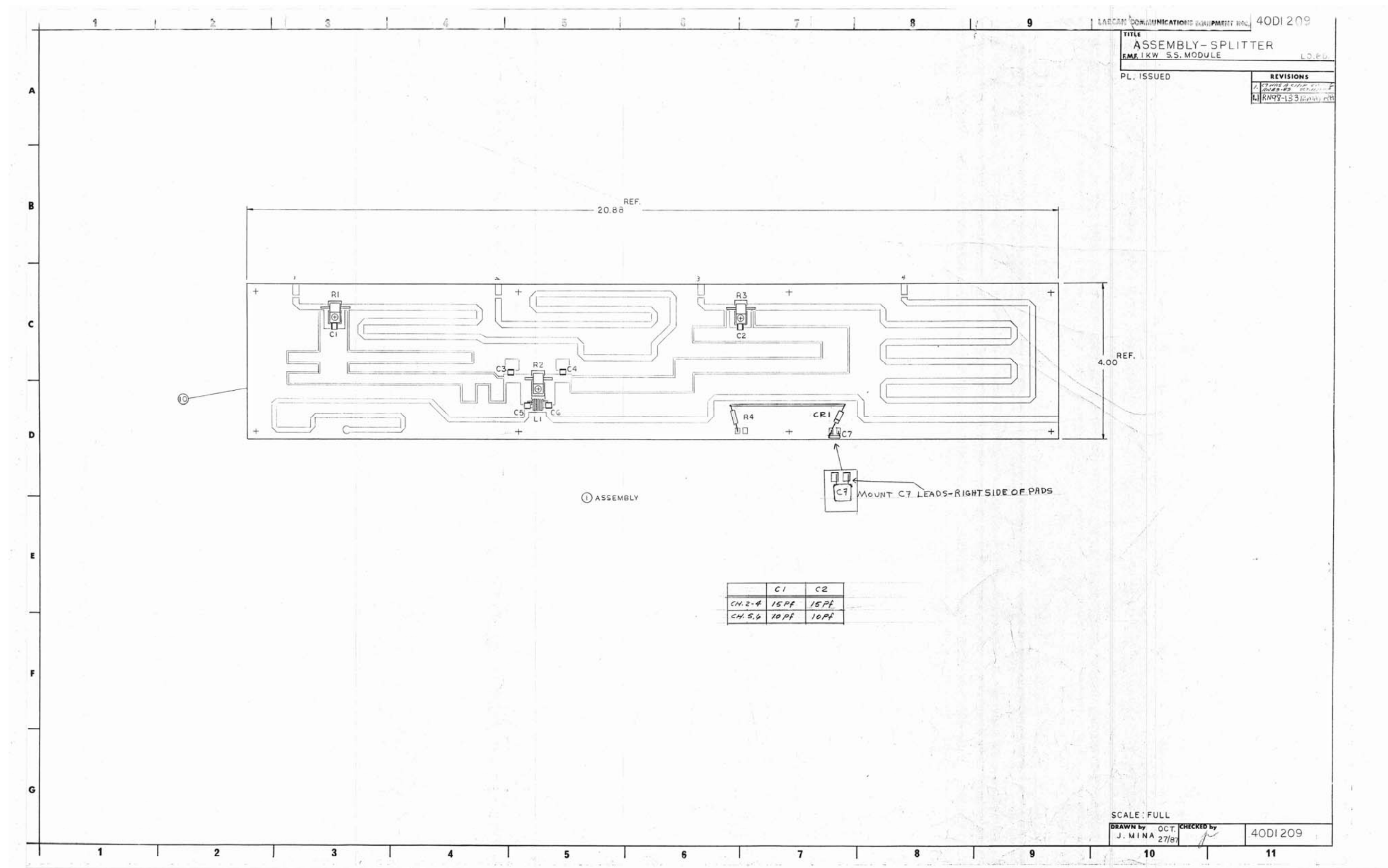
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**POWER AMPLIFIER 1KW LOW BAND 40D1137G1,2**



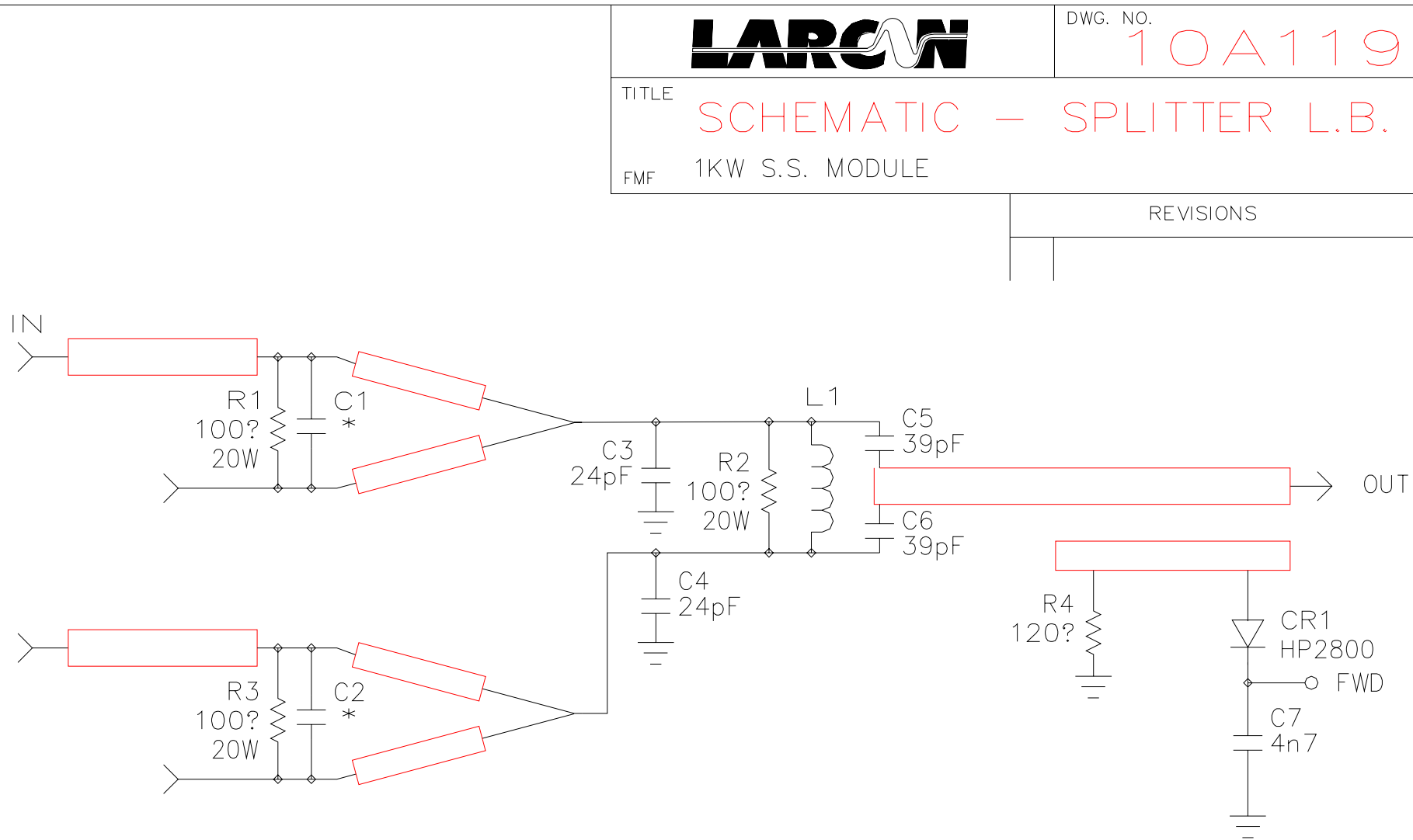
### Figure 3 Module Schematic 20B1502 rev 0

**POWER AMPLIFIER 1KW LOW BAND 40D1137G1,2**



**Figure 4 Four Way Input Splitter Assembly 40D1209 sht 1 rev 1.1**

**POWER AMPLIFIER 1KW LOW BAND 40D1137G1,2**



**Figure 5 Single Stage PA Schematic 10A1198 rev 0**

# POWER AMPLIFIER 1KW LOW BAND 40D1137G1,2

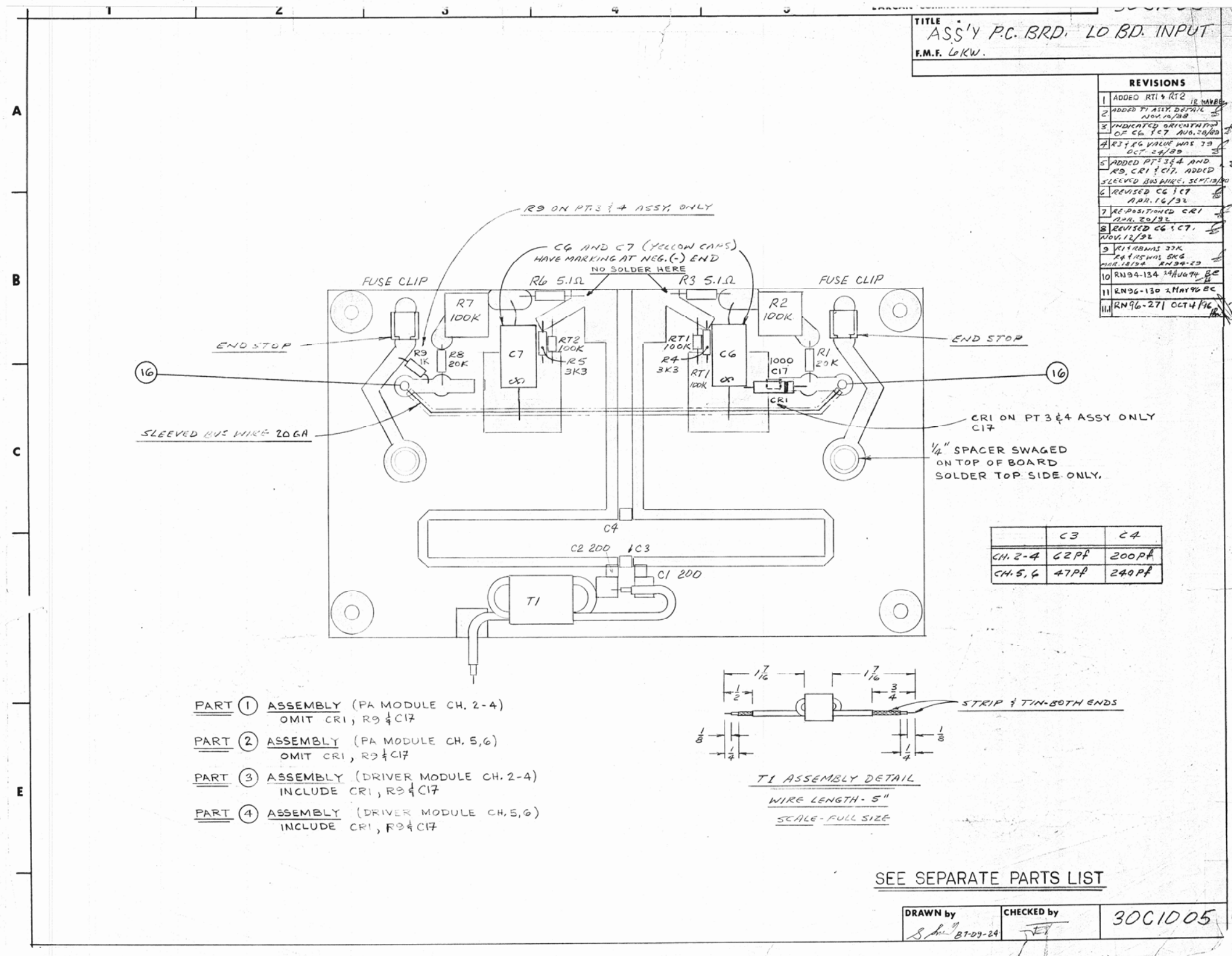


Figure 6 Input Board Assembly 30C1005 rev 11.1

POWER AMPLIFIER 1KW LOW BAND 40D1137G1,2

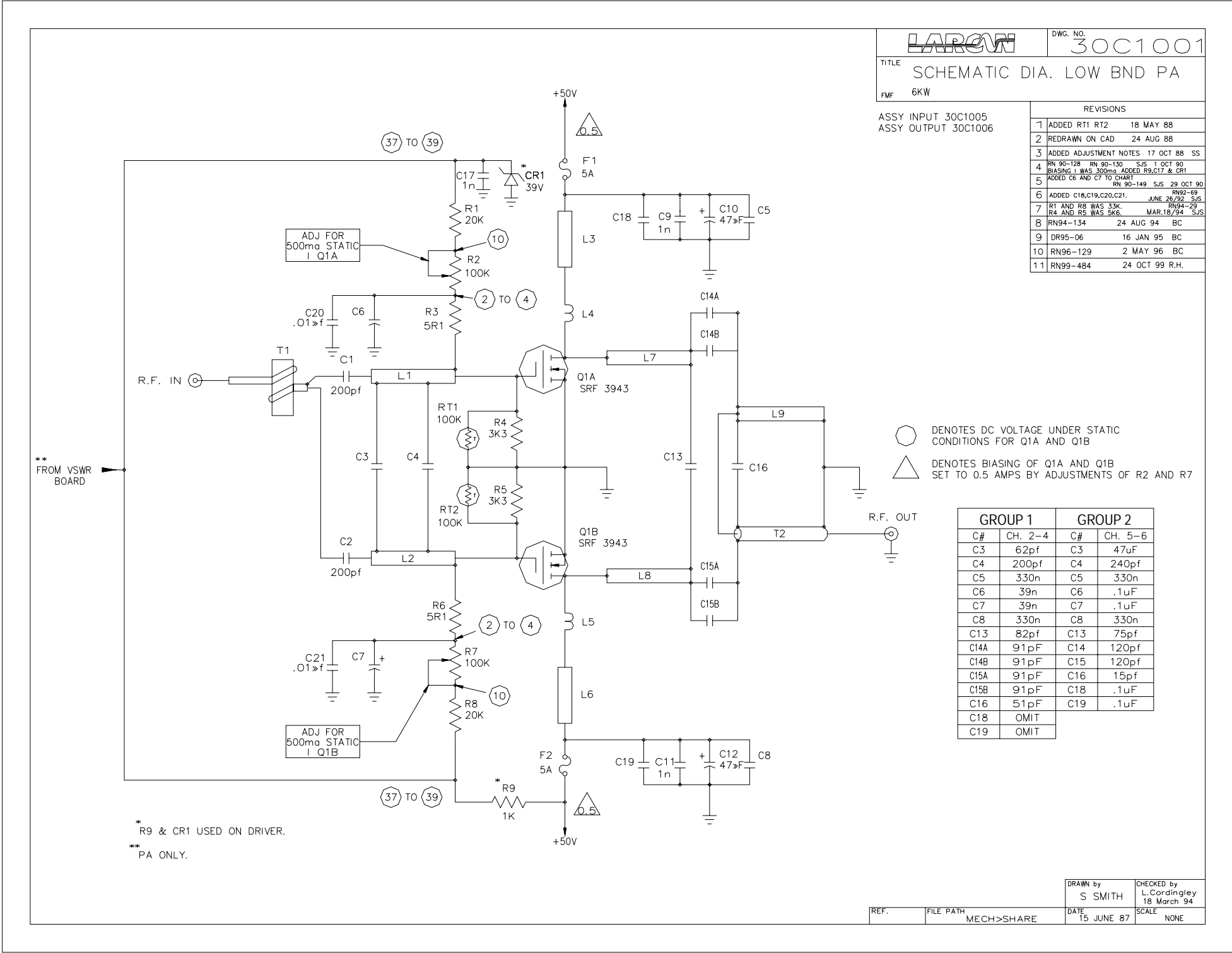


Figure 7 Single Stage PA Schematic 30C1001 sht 1 rev 11



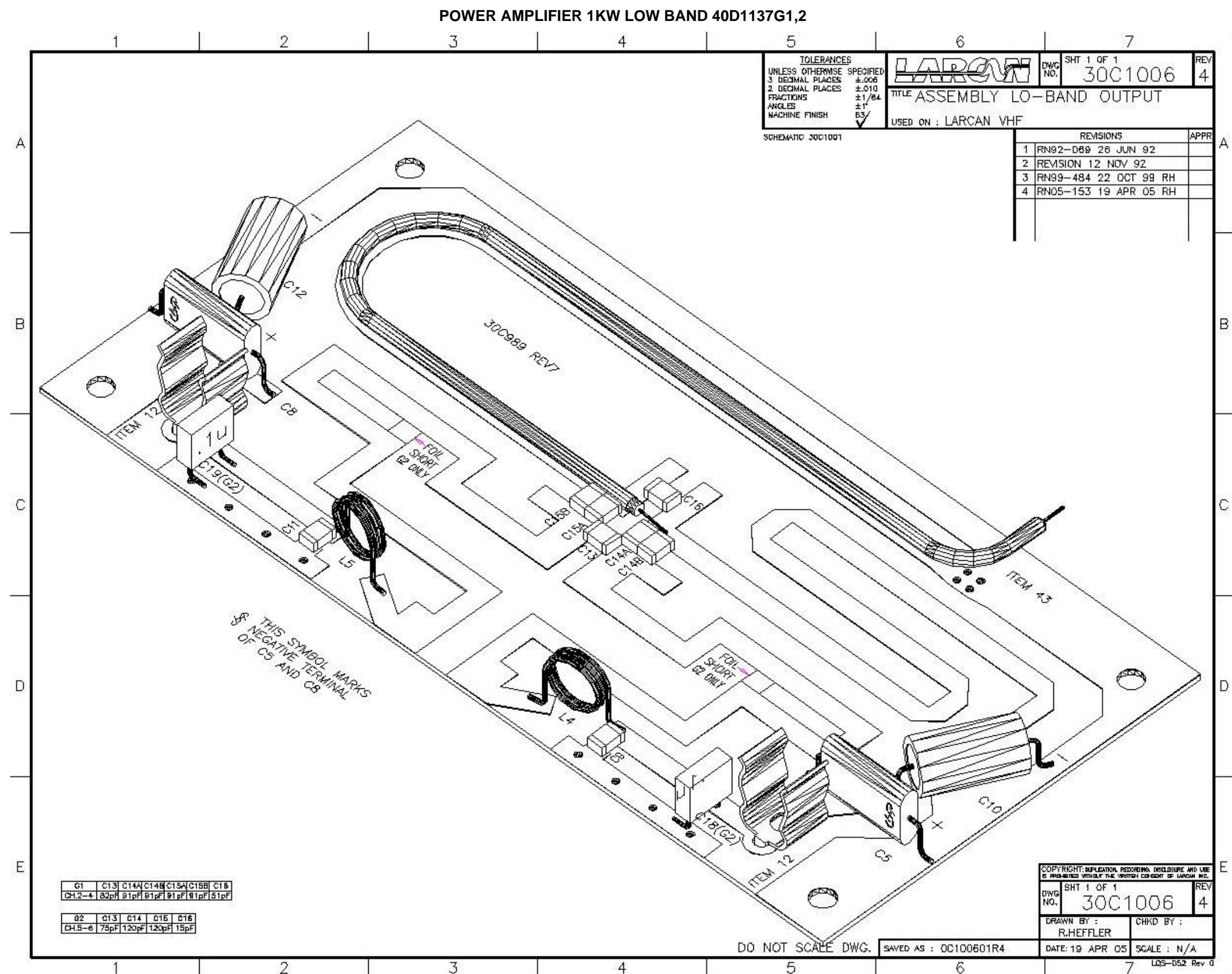


Figure 8 Output Board Assembly 30C1006 sht 1 rev 4



POWER AMPLIFIER 1KW LOW BAND 40D1137G1,2

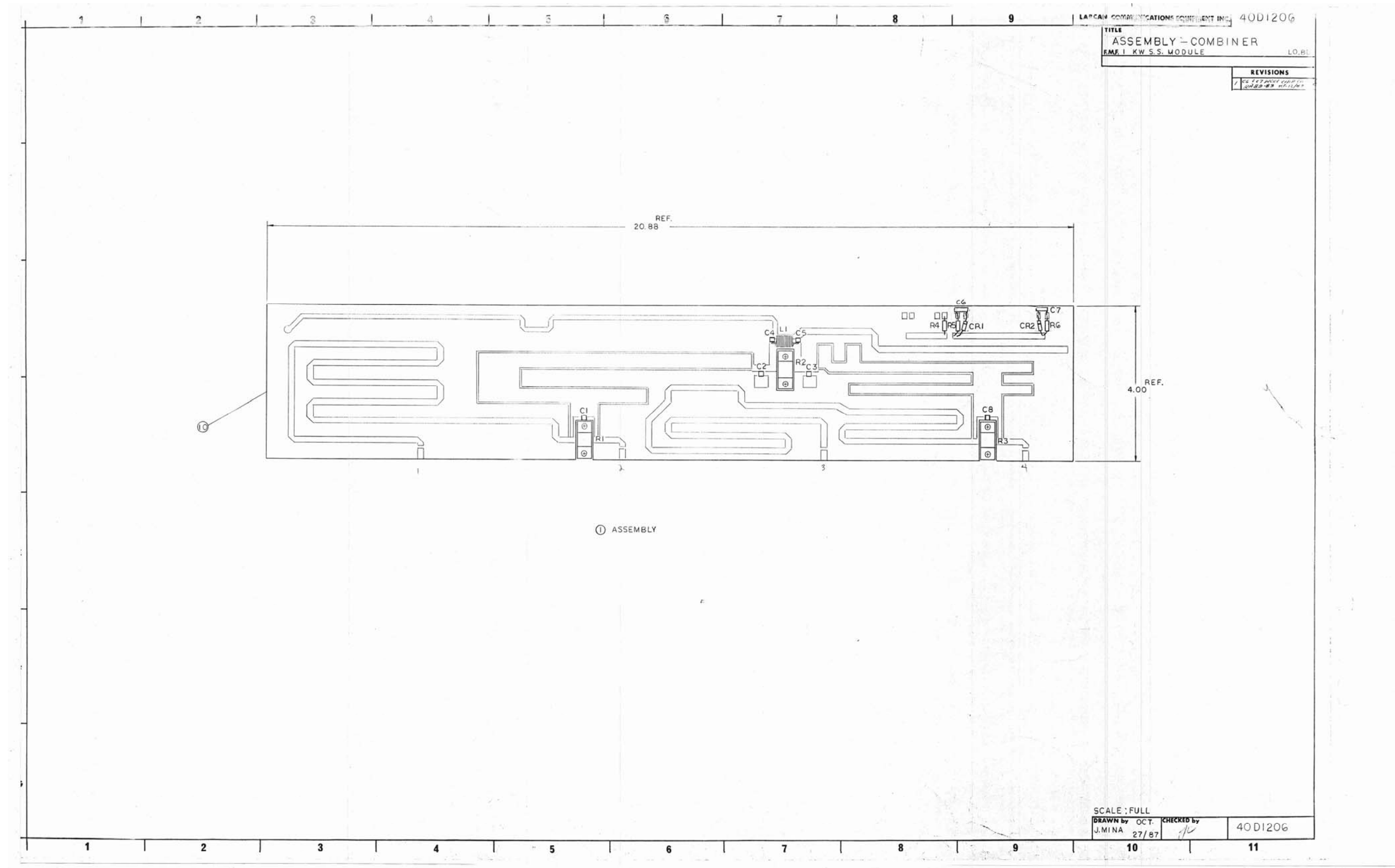
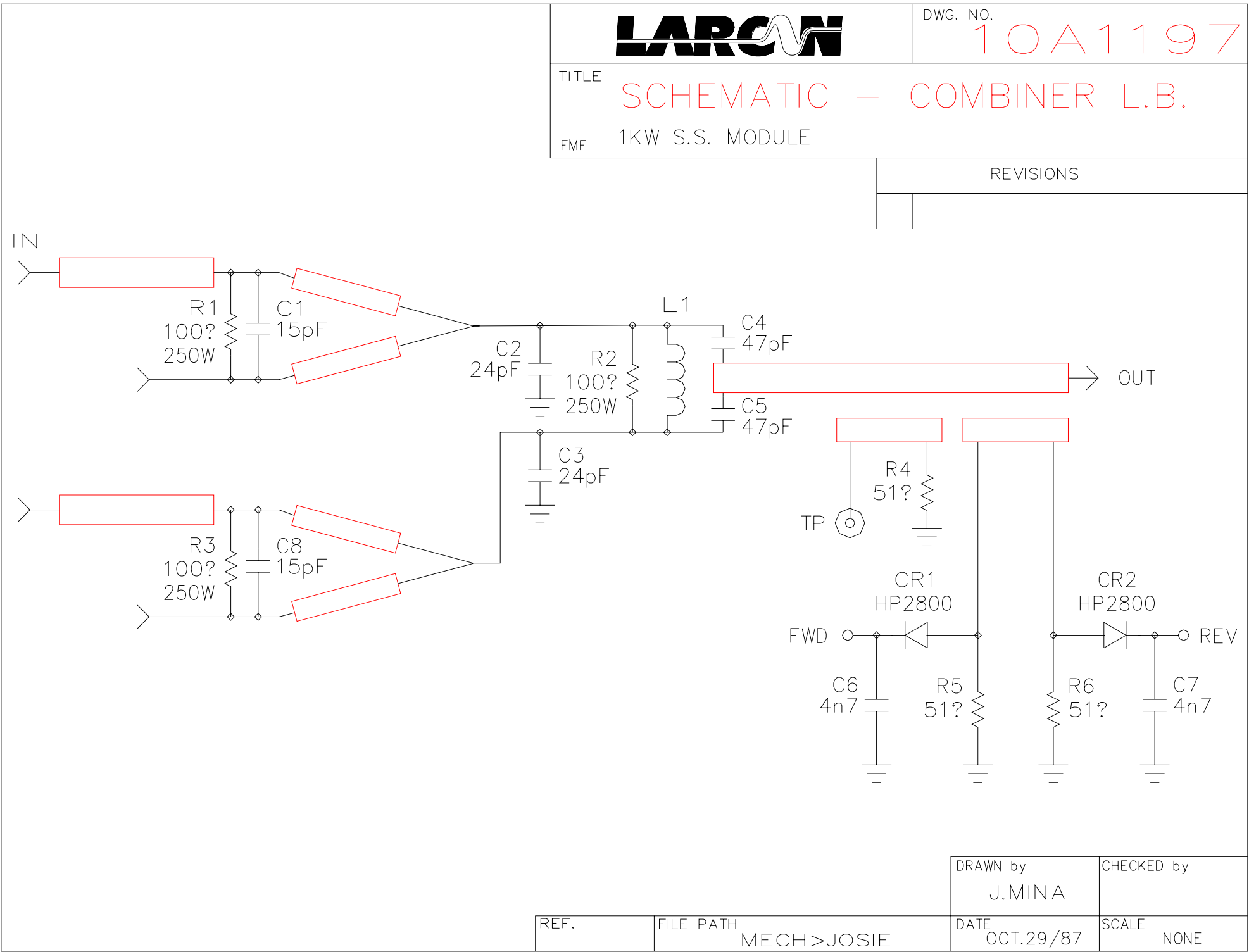


Figure 9 Four Way Combiner Assembly 40D1206 sht 1 rev 1

**POWER AMPLIFIER 1KW LOW BAND 40D1137G1,2**



**Figure 10 Four Way Combiner Schematic 10A1197 rev 0**

Schematic diagram of the VSWR Control Board (30C1418) showing component locations and assembly instructions.

**TOLERANCES**

UNLESS OTHERWISE SPECIFIED	
3 DECIMAL PLACES	±.005
2 DECIMAL PLACES	±.010
FRACTIONS	±1/64
ANGLES	±1°
MACHINE FINISH	63

**LARCAN**

DWG NO. 20B1594A1 REV 3.1

SHT 1 OF 1

TITLE ASSEMBLY - VSWR CONTROL BOARD

USED ON : VHF 1kW AND 1.5kW PA MODULES

ALL DIMENSIONS ARE IN INCHES UNLESS NOTED OTHERWISE

REVISIONS

REV	DESCRIPTION	DATE	BY	CHKD BY
1	DR92-26	21 SEPT 92	SJS	JET
2	DR95-73	20 SEPT 95	SS	JET
3	RN97-193	8 MAY 97	RH	JET
3.1	RN08-022	14 MAY 08	MPT	

SCHEMATIC: 30C1418

**Assembly Instructions:**

- SOLDER THESE TWO SPACERS UNDERSIDE ONLY
- SPACERS FAR SIDE TYPICAL
- DO NOT SOLDER THIS SPACER
- POSITION Q4 ON JIG OR DIRECTLY ON PA MODULE HEATSINK BEFORE SOLDERING TO PCB
- DO NOT SOLDER THIS SPACER

**Component Labels:** R10, R13, R29, C8, R4, U3, U4, C11, R28, R27, R26, LARCAN, R17, R19, R24, Q4, R25, C10, R21, R20, R22, R18, R23, Q3, R7, C9, C7, U1, R14, R8, C5, R6, R1, R12, CR1, U2, R15, R16, R11, R9, R5, J1, REV/3.1, 20B1594, 1, 14

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DWG NO. 20B1594A1 REV 3.1

SHT 1 OF 1

DRAWN BY : S. SMITH

CHKD BY : JET

DATE: MAR 90

SCALE : 1/1

NEXT ASSY:

DO NOT SCALE DWG.

SAVED AS: 0B1594A1R3\_1.dwg

QOS-052 Rev 1

PUB96-38 Rev 2

# POWER AMPLIFIER 1KW LOW BAND 40D1137G1,2

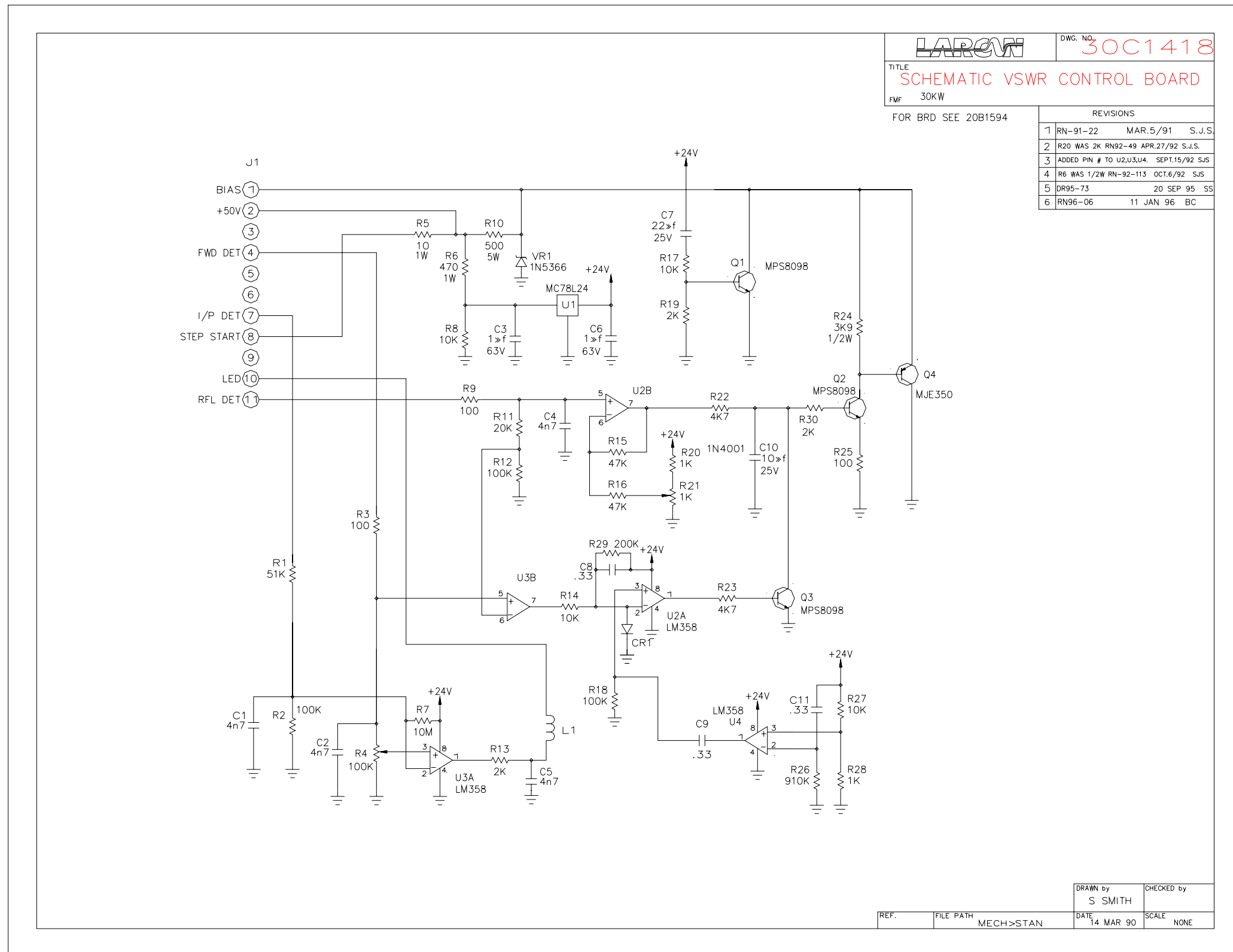


Figure 12 VSWR Protection Board Schematic 30C1418 sht 1 rev 6